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| **Course Name:** | **Automation and Control System** | **Semester:** | **V** |
| **Date of Performance:** | **11/09/2024** | **Batch No:** | **B1** |
| **Faculty Name:** | **Prof. Shila Dande** | **Roll No:** | **16014022050** |
| **Faculty Sign & Date:** |  | **Grade/Marks:** | **\_\_\_ / 25** |

Experiment No: 5

Title: Implementation Timer Circuit

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| **Aim and Objective of the Experiment:** |
| 1. Study the timing diagram of On Delay Timer 2. Solve the assignment of Ton timer 3. Study the timing diagram of OFF Delay Timer 4. Solve the assignment of Toff timer 5. Study the timing diagram of Pulse Timer 6. Solve the timing diagram of Pulse Timer |

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| **COs to be achieved:** |
| CO4: Interface PLC using proper communication device |

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| **Theory:** |
| PLC timers instruction is used to activate or deactivate a device after a preset interval of time.  **Types of Timers available are:**  On-Delay timer (TON) Off-Delay timer (TOF) Retentive timer on (RTO)  **On-Delay Timer (TON)**  It is used when an action is to begin a specified time after the input becomes true.  Consider an example wherein a certain step in the manufacturing process is to begin 30 seconds after a signal is received from a limit switch. The 30 seconds delay is the ON-delay timer’s preset value.  The figure below shows a symbolic representation of the timer. |



The instruction mainly includes three status bits namely EN, TT, DN. Their significance is as follows:

**Enable (EN) Bit: -** The enable bit indicates the TON instruction is enabled

**Timer-Timing (TT) Bit: -**The timing bit indicates that a timing operation is in process.

**Done (DN) Bit: -**The done bit changes state whenever the accumulated value reaches the preset value.

**Accumulator (ACC) Bit: -**The accumulated value specifies the number of milliseconds that have elapsed since the TON instruction was enabled.

**Preset (PRE) Bit: -** The preset value specifies the value (1msec units) which the accumulated value must reach before the instruction sets the .DN bit.

# OFF-Delay Timer:

Consider an example where the contents of a storage tank are to transfer to further process. When the low level is detected by level switch the outlet valve is to be closed. To allow entire contents to drain out, some time delay is needed as the level switch is installed slightly above the tank bottom level. This can be achieved by using off delay timer.

Consider an example that, there is a Low level switch to a tank, and we have to close the drain valve of the tank after 5 second delay when low level is reached. In this case this 5 seconds delay can be given using off delay timer as we have to close the drain valve after delay.

The figure below shows a symbolic representation of the off delay timer.

The instruction mainly includes three status bits namely EN, TT, DN. Their significance is as follows:

**EN-Enable Bit:** - The enable bit indicates the TOF instruction is enabled.

**TT-Timer-Timing Bit:** - The timing bit indicates the timing operation is in process.

**DN- Done Bit:** - The done bit changes state whenever the accumulated value reaches the preset value.

**ACC- Accumulator Bit:** - The accumulated value specifies the number of milliseconds that have elapsed since the TOF instruction was enabled.

**Pre-Preset Bit:** - The preset value specifies the value (1msec units) which the accumulated value must reach before the instruction clears the DN bit.

# Theory Introduction

Each manufacturer of PLC systems has own style of writing the instructions. Different PLCs has different instruction sets but even some common basic instructions are shared by all the PLCs. All manufacturers give different software packages for programming PLCs. Ladder is most commonly used programming language. Prior to PLCs, relay logic was used in industry. Ladders were developed to mimic or imitate relay logic.

Relay Logic / Instructions

A relay is simple magnetic device which acts as a control switch.

When the switch is on, current will flow through the coil on iron piece. This iron core acts a electromagnet and due to the magnetic field upper contact gets attracted towards lower one and circuit gets completed, allowing current to flow from load.





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| **Circuit Diagram/ Block Diagram:** |
| http://plc-coep.vlabs.ac.in/images/timing%20diagram_Ton.jpg  http://plc-coep.vlabs.ac.in/images/timing%20diagram_Toff.jpg |

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| **Stepwise-Procedure:** |
| **Develop an application using On-Delay Timer**  In this experiment the on delay timer will be tested for its functionalities using Simulator. Following bits of the timer are to be observed.   1. Initialising bit “ON” in this case. 2. Enable bit “T\_en” 3. Done bit “T\_dn” 4. Timer timing bit “T\_tt” 5. Preset value needs to be entered by the user. 6. While configuring the timer the default time is 1 mS. Select appropriate preset value as per the need of the application. 7. To test the EN, DN, and TT bits;configure the timer by right clicking anywhere on the timer block. Submit tag and preset value. Observe the bit status in Run mode when input a is toggled again.   **Develop an application using Off-Delay Timer**  The configuration of off delay timer is same as 'on delay timer'.  A typical difference can be observed in the operation (in Run mode) .  When the q bit is energised the output DN bit goes high. The timer starts only after toggling the initialisation bit again.  Pulse Timer:  In PLC programming, a pulse timer is a triggerable event timer that generates a fixed-duration output pulse when its input turns on. In a PLC the Pulse Timer is commonly known as a PT timer. The Pulse Timer creates an output PULSE with a pulse duration equal to that of the preset time value. In simple terms, the TP timer output is ON when the timer is running and is OFF all other times. |

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| **Lab Simulation:** |
| VLAB:      PLC: |

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| **Post Lab Subjective/Objective type Questions:** |
| 1. **Ton stands for**    1. Off delay timer    2. Retentive timer    3. On delay timer   **Answer: On delay timer**  **2) Ton timer is used when action is expected to be delayed**   1. True 2. False 3. Not always true   **Answer: True**  **3) Which of the following bit is used to start the timer operation**   1. TT 2. DN 3. EN   **Answer: EN**  **4) If the preset value is 2000, for a 1ms time base timer, the delay provided is**   1. 20 sec 2. 2 sec 3. 200 ms   **Answer: 2 sec** 5) Which bit of timer ensures that the timing process is going on  1. TT 2. DN 3. EN   **Answer: TT** The main difference between a Ton and a Toff timer is that  * 1. Toff can maintain the accumulated time on loss of logic continuity   2. Toff timer begins timing when logic continuity to the rung is lost   3. Ton can maintain the accumulated time on loss of logic continuity   **Answer: Toff timer begins timing when logic continuity to the rung is lost.** DN bit for Toff timer is initially high when the program is switched to run mode after downloading  * 1. True   2. False   3. Can’t say   **Answer: True** The done bit changes state whenever  * 1. the timer timing value reaches the preset value   2. the accumulated value reaches the timer timing value   3. the accumulated value reaches the preset value   **Answer: the accumulated value reaches the preset value** Toff is used when action is not expected after specific delay  * 1. True   2. False   3. Can’t say   **Answer:False**  **5) In off delay timer the status of TT bit is same as**  a) Rung condition IN bit  b) EN bit  c) DN bit  **Answer:Rung condition IN bit** |

**Signature of faculty in-charge with Date:**

**Conclusion:**

In this experiment, we learned about Delay Timers. We implemented T-ON and T-OFF timers using Vlab and TIA software and PLC hardware.